REMARKS

Claims 1-32 are pending in the application. The Examiner rejected claims 1-32 in the above mentioned Office Action.

Claim Rejections Under 35 U.S.C. §102

Claims 1-32 have been rejected under 35 U.S.C. §102(b) as being anticipated by Brisse. Applicant respectfully disagrees. Independent claims 1, 9, 17 and 25 include limitations neither disclosed nor suggested by Brisse.

As to claims 1 and 17, the Examiner stated that Brisse discloses all limitations of these claims on page 2 in the paragraphs before the 'Brief Description of the Drawings.' Applicant respectfully disagrees. According to claims 1 and 17, a method for handling a module or a memory module within a computer system comprises analyzing an error that occurred when the system accessed the module. The module itself comprises non-volatile memory section. After analyzing a memory error that occurred during operation of the system, a log is created and stored in the non-volatile section of the respective module in which the error occurred. Thus, this log can be retrieved if the module is removed from the system and the log will inform, for example, a vendor handling the module when the error occurred and what type of error occurred, etc. Thus, the vendor will immediately be informed about the status of the respective module and be in a better position to decide what has to be done to repair the module. Furthermore, the method allows to easily create statistics about certain products and their failure rate, etc.

Brisse discloses a system consisting of a motherboard comprising memory modules placed in memory module slots and a chip set for coupling the memory modules with the system. Page 2 of Brisse cited by the Examiner merely discloses that the system can store data in an error detection signal in a register in the chip set. However, Brisse neither discloses nor suggests that such a register is non-volatile. Moreover, such a register is not part of the respective memory module in which the respective error occurred. Thus, whenever the memory module is removed and shipped to a vendor, there will be no information available regarding the error that occurred within the respective module.

Brisse further discloses the use of ECC memory modules. An ECC memory module has the capability of correcting errors in a similar but advanced way as a parity bit does by using designated additional storage area. However, this additional storage area is also random access memory and not non-volatile memory. Also, ECC uses a special algorithm to encode information in a block of bits that contains sufficient detail to permit the recovery of a single bit error in the protected data. Unlike parity, which uses a single bit to provide protection to eight bits, ECC uses larger groupings: 7 bits to protect 32 bits, or 8 bits to protect 64 bits. There are special ECC memory modules designed specifically for use in ECC mode. However, the ECC mode is controlled through the motherboard, namely the chip set as shown in Fig. 1 of Brisse. Thus, ECC memory modules do not provide for a non-volatile memory area. Furthermore, ECC modules do not store a log containing information about an error that occurred within a memory module but rather use a mechanism of automatically correcting an error that occurred during operation of the module. Thus, an operator of an ECC module will never know that an error actually occurred as it is automatically corrected. As explained above, the present invention concerns a completely different problem and, thus, uses a completely different approach. According to the present invention, whenever an error occurred that affects a module in a way that it will not operate properly, this error is stored in a non-volatile area of the module in form of a log entry for later retrieval even if the module is removed from the system.

Independent claims 9 and 25 include the same limitations with respect to this non-volatile memory within a module as independent claims 1 and 17. Thus all above presented arguments also apply to these independent claims. Therefore, Brisse does not anticipate these claims.

The dependent claims include all the limitations of the respective independent claims to which they refer to. Thus these claims are patentable at least to the extent of the respective independent claims. However, because Brisse does not disclose imporatant limitations of the independent claims as discussed above and is therefore not relevant art, Applicants would like to defer any discussion of patentability with respect to these claims at this point.

SUMMARY

In light of the above remarks, reconsideration and withdrawal of the outstanding rejection is respectfully requested. Applicant further requests to defer any necessary amendment of the drawings until allowance of the claims. Early notice of the allowance is earnestly solicited. Should the Examiner have any questions, comments or suggestions in furtherance of the prosecution of this application, the Examiner is invited to contact the agent of record by telephone or facsimile. If there are any fees due with the filing of this Response, including any fees for an extension of time, Applicants respectfully Petition the Commissioner for such an extension and direct that any and all fees be charged to Baker Botts L.L.P., Deposit Account No. 02-0383, *(formerly Baker & Botts, L.L.P.,)* Order Number 016295.0693.

Respectfully submitted,

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